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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/205,086	12/04/98	BOGIN Z	42390.P5549

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EXAMINER	
ELMORE, R	
ART UNIT	**PAPER NUMBER**
2187	7

DATE MAILED: 07/17/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/205,086	BOGIN ET AL.	
	Examiner	Art Unit	
	REBA I. ELMORE	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 March 2001* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28 and 38-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28 and 38-49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

DETAILED ACTION

1. Claims 1-28 and 38-49 are presented for examination. Claims 29-37 have been cancelled by the amendment filed March 26, 2001.

Specification

2. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections

3. The rejection of claims 1-28 as being anticipated by Atkinson is maintained. This rejection is updated to include the newly added claims 38-49.

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

5. Claims 1-28 and 38-49 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Atkinson.

Atkinson teaches the claimed invention including a memory which can be Extended Data Out Dynamic Access Memory (EDO DRAM) in a computer. The computer can be put in a suspend mode to save energy (e.g., see Figure 2A). When the computer is in the suspend mode a divide by two counter is used in the memory refresh logic to send the refresh signal to the EDO DRAM to maintain the memory (e.g., see Figure 3A and 3B). When in a normal mode of

operation the divide by two counter is not used, instead the regular counter in the refresh counter in the refresh logic is used to initiate refreshing the DRAM in the traditional methods (e.g., see col. 8, line 63 to col. 9, line 15).

As to claim 38-49, Atkinson teaches a refresh timing circuit as part of the system circuitry, the refresh timing circuit comprising:

a. An internal clock generator (e.g., see Figure 2A, elements 140);

b. A first counter coupled to the clock generator (e.g., see Figure 3A, element 300);

c. A storage register taught as part of the queue storage elements contained in the control logic (e.g., see col. 11, line 54 to col. 12, line 3) coupled to the clock generator and the counter; and,

d. A comparator is taught as part of element 300 of Figure 3A coupled to the clock generator, the counter and the storage register.

As to claim 39, Atkinson teaches the refresh timing circuit operates in a normal mode and a low power mode (e.g., see col. 13, lines 11-34).

As to claims 40-49, Atkinson teaches the first counter counts the number of clock pulses generated by the clock generator is inherent to the function of counters in refresh control circuitry. Atkinson also teaches a second counter as well as a first counter with the counters transmitting data as appropriate to the storage register whenever the refresh timing circuit is operating in the normal mode or a low power mode, the data representing the number of clock pulses counted by one of the counter since the occurrence of a previous memory refresh event. All of the elements are taught by Atkinson. As to the language concerning the counting of clock pulses by a counter, counters are common in refresh circuitry, they are necessary elements for

the refresh activities to take place. Atkinson teaches the hardware elements to the extent claimed and as refresh activities take place in the reference in both the normal and low power mode with different paths being used for these functions, the details claimed are inherent to the relationships therebetween the elements and are met by the reference. If the recited results of counting pulses, activating refresh timing circuit transitions for each mode or using comparator results are not inherent in Atkinson then this would mean the applicant has failed to recite one or more critical features of the present invention. ((In re Collier 158 USPE 266 (CCPA 1968 and Ex Parte Masham (BdPatApp&Int) 2 USPQ2d 1647).

Response to Applicant's Remarks

6. Applicant's arguments filed March 26, 2001 have been fully considered but they are not persuasive.

7. As to the remarks concerning the refresh logic not be incorporated within a memory controller, the claims use open ended 'comprising' language. There is no indication within the claim language as the whether the controller is considered a memory board containing the control logic circuitry, a single integrated circuit chip or any other particular physical arrangement. Without further defining within the claims what is meant by 'a memory controller comprising' this type of relationship cannot be given further patentable weight. Applicant has not claimed any details relating to the use of a 'pin' much less anything that precludes the given reference due to requiring 'an additional pin in order to trigger memory refreshes'. This same reasoning applies to the refresh timing circuitry comprising an internal clock generator.

8. In response to applicant's arguments that cite the use of the counters, registers and comparators, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

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Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reba I. Elmore, whose telephone number is (703) 305-9706. The examiner can normally be reached on M-TH from 7:30 a.m. to 6:00 p.m. EST.

If attempts to reach the examiner by phone fail, the art unit supervisor for 2187, Do Yoo, can be reached for general questions concerning this application at (703) 308-4908. Additionally, the fax phone for Art Unit 2187 is (703) 308-6606.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist at (703) 305-3800/4700.

Reba I. Elmore
Primary Patent Examiner
Art Unit 2187